

ABSTRACT OF THE DISCLOSURE

654,760

A nonvolatile memory in the form of a flash EEPROM with high density and low cost. A vertical MOS transistor is formed in well etched into a semiconductor substrate, the substrate having a buried layer of doped material of a first conductivity type acting as the channel region. Source and drain regions of this transistor comprise second conductivity type layers doped in the substrate above and below the buried layer. A thin gate oxide or oxide-nitride-oxide (ONO) layer is formed in the well and a floating gate of polysilicon is formed over the gate oxide. A layer of oxide or ONO is formed over the floating gate, and a second polysilicon or metal layer is used to fill the well to form the control gate and word line. A bit line is formed of a layer of metal or polysilicon deposited over an insulating layer on top of the word line and makes contact with the drain of the vertical MOS transistor through a contact window formed adjacent the well.

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Ronald C. Fish

Ronald Craig Fish, President

30 Ronald Craig Fish a Law Corporation
Reg. No. 28,843